TRANSMITTAL OF APPEAL BRIEF (Small Entity)

Docket No.
MSS0007-US

In Re Application Of: **STERLING SMITH**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/663,755	September 17, 2003	NGUYEN, Hiep	00909	2816	3830

Invention: **INTERFACE CIRCUITRY FOR DISPLAY CHIP**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on:

☒ Applicant claims small entity status. See 37 CFR 1.27

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Signature

Dated: **June 26, 2006**

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on

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MSS0007-US PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	
STERLING SMITH	
Serial No.: 10/663,755	**Art Unit: 2816**
Filed: September 17, 2003	**Examiner: NGUYEN, Hiep**
For: INTERFACE CIRCUITRY FOR DISPLAY CHIP	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 35 U.S.C. §134 and C.F.R. §41.31, Appellant submits this Appeal Brief to appeal the Examiner's rejection of claims 1-14 in the final Office Action mailed March 26, 2006.

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I. REAL PARTY IN INTEREST

The named inventor has assigned all ownership rights in the pending application to MStar Semiconductor, Inc., 4F-1, No. 26, Tai-Yuan ST., ChuPei, HsinChu Hsien, Taiwan, R.O.C., which is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

The appellant, their legal representatives, and the assignee are not aware of any other pending appeals, interferences or judicial proceedings which may be related to, will directly affect or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 13 and 14 are to be cancelled. Claims 1-12 remain pending. The rejection of claims 1-12 is being appealed.

IV. STATUS OF AMENDMENTS

Claims 13 and 14 are cancelled in this application in response to the last Office Action dated February 1, 2006. The status of the claims in this application is as set forth above and in Appendix A.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The presently claimed invention relates to interface circuitries of a display chip such as a ADC (Analog/Digital Converter) chip or a display controller chip to improve the display quality of images. As noted in the background and Figure 1, in the conventional interface circuitry of Figure 1, the input noise level and the required input bandwidth vary significantly from different input modes and video source. In addition, aliasing from the input noise can affect detrimentally both the clamping level and the ADC output.

The interface circuitry of claim 1 includes an input node for receiving an analog image signal with a display resolution, a filter for processing said analog image signal and providing a processed image signal at an internal node, and a clamping circuit connected between said internal node and a reference level, wherein said filter provides a bandwidth adjustable in response to said display resolution such that the greater said display resolution, the greater said bandwidth, and wherein said clamping circuit is used to clamp said internal node at a clamping voltage with reference to said reference level during a clamping interval.

The interface circuitry of claim 7 includes an input node for receiving an analog image signal with a display resolution, a filter for processing said analog image signal and providing a processed image signal at an internal node, an ADC unit for converting said processed image signal into a digital image signal, and a clamping circuit connected between said internal node and a reference level, wherein said filter provides a bandwidth adjustable in response to said display resolution such that the greater said display resolution, the greater said bandwidth, and wherein said clamping circuit is used to clamp said iternal node at a clamping voltage with reference to said reference level during a clamping interval.

As recited in Figures 2 and 3 of the application, a low pass filter 24 comprises a variable resistor Rf connected between an input node 20 and an internal node 28 and a capacitor Cf connected between the internal node 28 and a ground node. The variable resistor Rf is utilized to provide different resistances based upon the display mode and required bandwidth. As stated in the paragraph bridging pages 6 and 7, the filter 24 provides a bandwidth, by adjusting the resistance of the variable resistor Rf, in accordance with the display mode.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are to be reviewed on appeal:

(1) Claims 13-14 under 35 U.S.C. §112, first paragraph;

(2) Claims 1, 3, and 4 under 35 U.S.C. §102(b) over the combination of Peterson et al. (US 5,926,217);

(3) Claims 1-4 and 13 under 35 U.S.C. §103(a) over the combination of Olmstead et al. (US 5,814,803) and Kanagawa et al. (US 6,366,866);

(4) Claims 5-6 under 35 U.S.C. §103(a) over the combination of Peterson et al. and Kwon et al. (US 6,724,245); and

(5) Claims 7-12 and 14 under 35 U.S.C. §103(a) over the combination of Obie et al. (5,038,096), Olmstead et al., Kwon et al., and Kanagawa et al.

VII. ARGUMENT

A. The 35 U.S.C. §112, first paragraph rejection of claims 13 and 14 are now moot due to the cancellation of claims 13 and 14

Applicant has cancelled claims 13 and 14 at shown in Appendix A. Thus, the rejection of claims 13-14 under 35 U.S.C. §112, first paragraph is now moot.

B. The 35 U.S.C. §102 rejection of claims 1, 3, and 4 based on Peterson et al. is improper and should be withdrawn

Independent claim 1 relates to interface circuitry for a display chip including, among other things, an input node for receiving an analog image signal with a display resolution, a filter for processing said analog image signal and providing a processed image signal at an internal node, and a clamping circuit connected between said internal node and a reference level, wherein the filter provides a bandwidth adjustable in response to said display resolution such that the

greater said display resolution, the greater said bandwidth, and wherein the clamping circuit is used to clamp the internal node at a clamping voltage with reference to said reference level during a clamping interval.

As recited in Figures 2 and 3 of the application, a low pass filter 24 comprises a variable resistor Rf connected between an input node 20 and an internal node 28 and a capacitor Cf connected between the internal node 28 and a ground node. The variable resistor Rf is utilized to provide different resistances based upon the display mode and required bandwidth. As stated in the paragraph bridging pages 6 and 7, the filter 24 provides a bandwidth, by adjusting the resistance of the variable resistor Rf, in accordance with the display mode.

It is respectfully submitted that Peterson et al. fail to teach or suggest at least a filter that "provides a bandwidth in response to said display resolution such that the greater said display resolution, the greater said bandwidth," as recited in independent claim 1. Peterson et al. only describe an adjustable low pass filter, but there is no teaching or suggesting that the low pass filter provides a bandwidth in response to the display resolution. Further, since Peterson et al. fail to teach or suggest this feature of claim 1, it would not have been inherent, as asserted by the Examiner, that "the greater the bandwidth, the greater the display resolution is," noting that this portion of the claim is associated with the adjustable filter that is responsive to the display resolution. Therefore, Applicant respectfully traverses the §102(e) rejection of claims 1, 3, and 4 by Peterson et al.

C. The 35 U.S.C. §103 rejection of claims 1-4 and 13 based on a combination of Olmstead et al. and Kanagawa et al. is improper and should be withdrawn

To establish a prima facie case of obviousness, there must be (1) some suggestion or motivation (either in the references themselves or in the knowledge generally available to one of ordinary skill in the art) to modify the reference or to combine reference teachings to achieve the claimed invention, and (2) the prior art must teach or suggest all the claim limitations. MPEP §2143.

The Federal Circuit has recently elaborated on the necessity of clear articulation of the motivation for combining elements disclosed in different prior art references. As noted by the Federal Circuit,

> [m]ost inventions arise from a combination of old elements and each element may often be found in the prior art. However, mere identification in the prior art of each element is insufficient to defeat the patentability of the combined subject matter as a whole. Rather, to establish a prima facie case of obviousness based on a combination of elements disclosed in the prior art, the Board must articulate the basis on which is concludes that it would have been obvious to make the claimed invention. In practice, this requires that the Board explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious....
>
> When the board does not explain the motivation, or the suggestion or teaching, that would have led the skilled artisan at the time of the invention to the claimed combination as a whole, we infer that the Board used hindsight to conclude that the invention was obvious.

In re Leonard R. Kahn, Slip Op. 04-1616 (Fed. Cir. 2006) (internal citations omitted)(emphasis added).

As noted above, Applicant claims a interface circuitry for a display chip including, among other things, an input node for receiving an analog image signal with a display resolution,

a filter for processing said analog image signal and providing a processed image signal at an internal node, and a clamping circuit connected between said internal node and a reference level, wherein the filter provides a bandwidth adjustable in response to said display resolution such that the greater said display resolution, the greater said bandwidth, and wherein the clamping circuit is used to clamp the internal node at a clamping voltage with reference to said reference level during a clamping interval, as recited in independent claim 1.

Page 3 of the final Office Action makes the following conclusiory remarks about the combination of Olmstead et al. and Kanagawa et al.:

> Regarding claim 1, figure 10A of Olmstead shows an interface circuitry of a display chip comprising: an input code (CCD) for receiving an analog input signal with a display mode; a filter (274); a clamping circuit (S1). Figure 10A of Olmstead does not show that the filter is adjustable. Figure 3 of Kanagawa shows an adjustable filter for adjusting the bandwidth of the analog input signal according to the display mode. Therefore, it would have been obvious to those skilled in the art to replace the fixed filter of Olmstead with the adjustable taught by Kanagawa for adjusting the bandwidth according to the display mode and it is inherent that the greater the bandwidth, the greater the display resolution is (see USPats. 3,908,193; 3,983,328; 4,676,105; 5,l28,549; 5,394,750; 6,497,666; 6,677,882 and 6,681,065).

As admitted by the Examiner, Olmstead et al. fails to teach or suggest a filter that "provides a bandwidth in response to said display resolution such that the greater said display resolution, the greater said bandwidth," as recited in independent claim 1. To support the obviousness rejection, the Examiner relied on Kanagawa et al. that comprises an adjustable filter. The adjustable filter of Kanagawa et al., however, does not include the function of the filter of claim 1. For example, the noise filter 21 of Kanagawa et al. includes a CR filter 211 coupled to receive X data signal X0 and a CR filter 212 couple to receive Y data signal Y0. As described in

column 4, lines 6-17, values of resistors 2111 and 2121 (of CR filters 211 and 212, respectively) are adjustable is response to noise involved in the X data signal and Y data signal, not resolution mode. Accordingly, in any combination of Olmstead et al. and Kanagawa et al., it would not have been obvious for one skilled in the art to achieve the circuitry of claim 1 because none of Olmstead and Kanagawa discloses the feature of the filter recited in claim 1. Moreover, the other eight cited patents (Patent Nos. 3,908,193, 3,983,328, 4,676,105, 5,128,549, 5,394,750, 6,497,666, 6,677,882, and 6,681,065) do not relate to an interface circuitry of a display chip. Therefore, their combinations with Peterson do not support the obviousness rejection. Consequently, the Examiner has failed to make a prima facie case of obviousness.

For at least these reasons, the §103 rejection of claims 1-4 based on a combination of Olmstead et al. and Kanagawa should be withdrawn. Furthermore, as claim 13 has been cancelled in the Amendment (see Appendix A), the rejection of this claim is considered moot.

D. The 35 U.S.C. §103 rejection of claims 5-6 based on a combination of Peterson et al. and Kwon et al. is improper and should be withdrawn

At least due to their dependency from patentable independent claim 1, it is respectfully submitted that dependent claims 5 and 6 should be also patentable. Accordingly, the rejection of claims 5-6 in the combination of Peterson et al. and Kwon et al. should be withdrawn.

E. The 35 U.S.C. §103 rejection of claims 7-12 and 14 based on a combination of Obie et al., Olmstead et al., Kown et al., and Kanagawa et al. is improper and should be withdrawn

Independent claim 7 relates to interface circuitry for a display chip that has features similar to independent claim 1. For example, the interface circuitry of claim 7 includes an input node for receiving an analog image signal with a display resolution, a filter for processing said analog image signal and providing a processed image signal at an internal node, and a clamping

circuit connected between said internal node and a reference level, wherein the filter provides a bandwidth adjustable in response to said display resolution such that the greater said display resolution, the greater said bandwidth, and wherein the clamping circuit is used to clamp the internal node at a clamping voltage with reference to said reference level during a clamping interval.

Page 4 of the final Office Action makes the following conclusiory remarks about the combination of Obie et al., Olmstead et al., Kwon et al., and Kanagawa et al.:

> Figure 1 of Obie does not show a clamping circuit connecting between said internal node and a reference level and the filter is adjustable. Figure 10A Olmstead shows an interface circuitry of a display chip comprising a clamping circuit (131) connecting between said internal node and a non zero reference level for establishing a precise reference for each pixel before video bump occurs (col. 12, lines 47-57). Figure 3 of Kanagawa shows an adjustable low-pass filter (211) for eliminating high frequency noise. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to implement the clamping by Peterson into the circuit of Obie for establishing a precise reference for each pixel before video bump occurs and to replace the fixed video filter (112) with the adjustable filter (211) taught by Kanagawa for eliminating high frequency noise.

With respect to the obviousness rejection of independent claim 7, the Examiner asserted that Obie et al. fail to teach or suggest a clamping circuit, but relied on a clamping circuit of Olmstead and adjustable filter of Kanagawa to complete his reason for rejection. For Olmstead et al., as shown in Figure 10A, the clamping circuitry (composed of amplifiers A1 and A2 and switches S1 and S2) is not located between an internal node of the low pass filter 274 and a reference level, as recited in independent claim 7. Indeed, the clamping circuit is coupled to the output of the low pass filter 274. For Kanagawa et al., as argued above, values of resistors 2111 and 2121 (of CR filters 211 and 212, respectively) are adjustable in response to noise involved in

the X data signal and Y data signal, not resolution mode, as recited in independent claim 7. Accordingly, Applicant respectfully submits that it would not have been obvious for one skilled in the art to combine Obie et al., Olmstead et al., and Kanagawa et al. to achieve the circuitry of independent claim 7 for the differences mentioned above.

Accordingly, the §103 rejection of claims 7-12 based on the combination of Obie et al., Olmstead et al., Kwon et al., and Kanagawa et al. should also be withdrawn. Furthermore, the rejection of claim 14 is now moot as claim 14 has been canceled in the Amendment.

F. Conclusion

For all of the above reasons, it is respectfully asserted that the pending claims of the present application are not anticipated and would not have been obvious to those of ordinary skill in the art. Accordingly, the Board should overturn the present rejections. Reversal of the pending rejections of record and allowance of the claims of this application are respectfully requested.

VIII. LISTING OF CLAIMS

(See Appendix A)

IX. EVIDENCE APPENDIX

(None.)

X. RELATED PROCEEDINGS APPENDIX

(None.)

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Respectfully submitted,

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Date: June 26, 2006

By: _____
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APPENDIX A

Listing of Claims:

1. (Previously Presented) An interface circuitry of a display chip, said interface circuitry comprising:

an input node for receiving an analog image signal with a display resolution;

a filter for processing said analog image signal and providing a processed image signal at an internal node; and

a clamping circuit connected between said internal node and a reference level;

wherein said filter provides a bandwidth adjustable in response to said display resolution such that the greater said display resolution, the greater said bandwidth,

wherein said clamping circuit is used to clamp said internal node at a clamping voltage with reference to said reference level during a clamping interval.

2. (Original) The interface circuitry as claimed in claim 1, wherein said filter comprises:

a variable resistor electrically connected between said input node and said internal node; and

a capacitor electrically connected between said internal node and a ground node.

3. (Original) The interface circuitry as claimed in claim 1, wherein said clamping circuit comprises a transistor connected between said internal node and said reference level.

4. (original) The interface circuitry as claimed in claim 3, wherein said transistor is configured with a drain connected to said internal node, a source connected to said reference level and a gate controlled by a clamping signal.

5. (Original) The interface circuitry as claimed in claim 1, wherein said clamping circuit comprises:

a variable resistor connected to said internal node; and

a transistor connected between said variable resistor and said reference level.

6. (Original) The interface circuitry as claimed in claim 5, wherein said transistor is configured with a drain connected to said variable resistor, a source connected to said reference level and a gate controlled by a clamping signal.

7. (Previously Presented) An interface circuitry of a display chip, said interface circuitry comprising:

an input node for receiving an analog image signal with a display resolution;

a filter for processing said analog image signal and providing a processed image signal at an internal node;

an ADC unit for converting said processed image signal into a digital image signal; and

a clamping circuit connected between said internal node and a reference level;

wherein said filter provides a bandwidth adjustable in response to said display resolution such that the greater said display resolution, the greater said bandwidth;

wherein said clamping circuit is used to clamp said internal node at a clamping voltage with reference to said reference level during a clamping interval.

8. (Original) The interface circuitry as claimed in claim 7, wherein said filter comprises:

a variable resistor electrically connected between said input node and said internal node; and

a capacitor electrically connected between said internal node and a ground node.

9. (Original) The interface circuitry as claimed in claim 7, wherein said clamping circuit comprises a transistor connected between said internal node and said reference level.

10. (Original) The interface circuitry as claimed in claim 9, wherein said transistor is configured with a drain connected to said internal node, a source connected to said reference level and a gate controlled by a clamping signal.

11. (Original) The interface circuitry as claimed in claim 7, wherein said clamping circuit comprises:

a variable resistor connected to said internal node; and

a transistor connected between said variable resistor and said reference level.

12. (Original) The interface circuitry as claimed in claim 11, wherein said transistor is configured with a drain connected to said variable resistor, a source connected to said reference level and a gate controlled by a clamping signal.

13.-14. (Cancelled)